What is claimed is:

1. An apparatus for decoding data, the apparatus comprising:

a bus;

hardware modules connected to the bus and configured to execute a decoding process; and

a processing unit connected to the bus, wherein the processing unit executes a decoding process by sending programmed signals to the hardware modules and responding to interrupts from the hardware components according to a set of programmed instructions.

2. The apparatus of Claim 1 further comprising a second bus connected to the processing unit and at least one of the hardware modules.

3. The apparatus of Claim 1, wherein the hardware modules comprise:

at least one hardware unit that decodes video data according to a video decoding method programmed into the processing unit; and

at least one audio hardware unit that decodes audio data according an audio decoding method programmed into the processing unit.

4. The apparatus of Claim 3, wherein the hardware modules retrieve audio data from the main memory unit before decoding.

5. The apparatus of Claim 1, wherein the hardware modules comprise:

a transformation unit that transforms the video data into pixel data; and

a motion compensation unit that performs interpolations using the pixel data and reference data from the main memory unit to create a reconstructed image.

6. The apparatus of Claim 1 further comprising an interface unit that receives compressed MPEG data, wherein the hardware modules comprise a variable length decoder unit that performs partial decompression of the bitstream.

7. The apparatus of Claim 6, wherein the variable length decoder unit sends an interrupt to the processing unit upon finding a startcode which triggers the decoding method.

8. The apparatus of Claim 1, wherein the processing unit executes the decoding process by serially activating certain ones of the hardware modules in accordance with a computer program.

9. The apparatus of Claim 1, wherein the processing unit comprises a first processor and a second processor, wherein the interrupt is programmatically mapped to at least one of the first and the second processors.

10. The apparatus of Claim 9 further comprising:
a local memory unit for the first processor; and
an engine for transferring data between the main memory unit and the local memory unit.

11. The apparatus of Claim 9, wherein the first processor is configured to handle video decoding and display control and the second processor is configured to handle audio decoding.

12. The apparatus of Claim 1, wherein the main memory unit stores video data and audio data separately.

13. The apparatus of Claim 1 further comprising a host interface unit that receives video and audio data, parses the data, and stores the video and audio data in the main memory unit.

14. The apparatus of Claim 1 further comprising an Assist hardware unit that receives interrupts generated by the hardware modules and forwards the interrupts to the processing unit.

15. The apparatus of Claim 14, wherein the Assist unit stores an arbitration scheme for the hardware modules.

16. The apparatus of Claim 15, wherein the arbitration scheme comprises prioritization of video data transfers over audio data transfers.

17. The apparatus of Claim 1 wherein the decoding process comprises variable length decoding, inverse quantization, inverse discrete cosine transform, and motion compensation that are executed by the different hardware modules in response to separate signals from the processing unit.

18. The apparatus of Claim 1, wherein the processing unit determines a decoding status, evaluates header parameters and checks for errors.

19. The apparatus of Claim 18, wherein the processing unit reads registers in different hardware modules, the registers indicating a current process state and presence of any errors.

20. The apparatus of Claim 19, wherein the processing unit reconfigures the hardware modules to generate correct data from incorrect data.

21. The apparatus of Claim 20, wherein the processing unit purges the error from the decoding process upon determining that the error is incorrigible.

22. The apparatus of Claim 1, wherein an interrupt from a hardware module in charge of motion compensation indicates that the decoding process is completed for a portion of an image.

23. The apparatus of Claim 1, wherein the processing unit sends signals to the hardware modules in an order dictated by a computer program, and wherein the decoding process is changeable by modification of the computer program.

24. The apparatus of Claim 1, wherein the hardware modules decode motion vectors in the data.

25. The apparatus of Claim 1, wherein the hardware modules perform data transformation by one of inverse quantization, arithmetic, saturation, mismatch control, and two-dimensional inverse discrete cosine transform.

26. The apparatus of Claim 25, wherein the two-dimensional inverse discrete cosine transform includes at least one of row-column decomposition and two-dimensional direct implementation.

27. The apparatus of Claim 1 further comprising a buffer associated with each of the hardware modules.

28. The apparatus of Claim 1, wherein the main memory unit is divided into cells according to a luminance indicator and a chrominance indicator of a field in a data frame.

29. The apparatus of Claim 1, wherein the apparatus is integrated as a system-on-chip system.

30. The apparatus of Claim 1, wherein the decoding process comprises interrupt signals generated by different hardware modules as each of the hardware modules completes its task.

31. The apparatus of Claim 1, wherein the hardware modules comprise components for decrypting input data.

32. An apparatus for video and audio decoding, the apparatus comprising:

a data bus;

hardware modules connected to the data bus, each of the hardware modules being configured to perform a discrete task; and

a processing unit connected to the data bus, wherein the processing unit executes a decoding process by activating the hardware modules in an order dictated by a computer program, and wherein the decoding process is changeable by modifying the computer program.

33. A method of decoding data, the method comprising:

establishing communications with a plurality of hardware modules, wherein each of the hardware modules is configured to perform a discrete task; and

activating the hardware modules in an order dictated by a computer program to execute a decoding process.

34. The method of Claim 33 further comprising:

determining a type of an input data;

identifying audio data in the input data;

identifying video data in the input data; and

directing the video input data to a video hardware component that is designed to process video data and directing the audio data to an audio hardware component that is designed to process audio data.

35. The method of Claim 33 further comprising:

determining a type of an input data;

identifying audio data in the input data;

identifying video data in the input data; and

sending the video signal to one of the hardware modules to store the input data in a video storage area and sending the audio signal to an audio storage area.

36. The method of Claim 33 further comprising sending a signal to one of the hardware modules to decrypt an input data stream.

37. The method of Claim 33, wherein the decoding process comprises:

extracting header information for a macroblock of the input data;

converting the macroblock into pixel data; and

generating a reconstructed image based on the pixel data by using motion compensation, wherein a motion compensation module that executes the motion compensation is reprogrammable for each macroblock.

38. The method of Claim 37, wherein the decoding process comprises retrieving data from a memory unit that is subdivided into sections according to luminance and chrominance.

39. The method of Claim 33, wherein the decoding process comprises prioritizing video data transfers over audio data transfers.

40. The method of Claim 33, wherein the decoding process comprises one or more of variable length decoding, inverse quantization, inverse discrete cosine transform, and motion compensation that are executed by the different hardware modules in response to separate signals.

41. The method of Claim 33, wherein different hardware modules process different macroblocks of data simultaneously.

42. The method of Claim 33 further comprising determining a decoding status and checking for errors.

43. The method of Claim 42 further comprising reconfiguring the hardware modules to generate a correct data from an incorrect data that is currently being processed, if an error is present.

44. The method of Claim 43 further comprising purging the error from the decoding process upon determining that the error is incorrigible.

45. The method of Claim 33, wherein the decoding process comprises decrypting input data.

46. A method of decoding data, the method comprising:

identifying a macroblock of data; and

sending a signal to a second hardware module to perform a second decoding process on the macroblock after receiving an interrupt from a first hardware module, the interrupt indicating completion of a first decoding process on the macroblock.

47. The method of Claim 46, wherein the first hardware module comprises a variable length decoder unit that decodes the macroblock's header information and a transformation unit that quantizes the macroblock's data, and the second hardware module comprises a motion compensation unit.

48. The method of Claim 46, wherein the first hardware module processes another macroblock while the second hardware module is processing the macroblock.

49. The method of Claim 46 further comprising decompression of the macroblock.

50. An apparatus for decoding data, the apparatus comprising:

a bus;

hardware modules connected to the bus and configured to execute a decoding process;

a processing unit connected to the bus; and

computer-readable instructions for the processing unit, wherein the computer-readable instructions map out which signals to issue in response to interrupts from the hardware modules.